

WHAT IS CLAIMED IS:

1 1. A data processor comprising:

2 an instruction execution pipeline comprising N processing
3 stages, each of said N processing stages capable of performing one
4 of a plurality of execution steps associated with a pending
5 instruction being executed by said instruction execution pipeline;

6 a data cache capable of storing data values used by said
7 pending instruction;

8 a plurality of architectural registers capable of
9 receiving said data values from said data cache;

10 bypass circuitry capable of transferring a first data
11 value from said data cache directly to a functional unit in one of
12 said N processing stages without first storing said first data
13 value in a destination one of said plurality of architectural
14 registers; and

15 a cache refill controller capable of detecting that a
16 cache miss has occurred at a first address associated with said
17 first data value, receiving a missed cache line from a main memory
18 coupled to said data processor, and causing said first data value
19 to be transferred from said missed cache line to said functional
20 unit.

1 2. The data processor as set forth in Claim 1 wherein said
2 cache refill controller is further capable of stalling said
3 instruction execution pipeline after said cache miss by halting
4 clock signals driving said instruction execution pipeline.

1 3. The data processor as set forth in Claim 2 further
2 comprising a clock controller coupled to said cache refill
3 controller and capable of generating said clock signals driving
4 said instruction execution pipeline, wherein said clock controller
5 stalls said instruction execution pipeline by halting said clock
6 signals in response to a command from said cache refill controller.

1 4. The data processor as set forth in Claim 3 wherein said
2 cache refill controller causes said first data value to be
3 transferred to said functional unit when said instruction execution
4 pipeline is stalled.

1 5. The data processor as set forth in Claim 4 wherein said
2 cache refill controller is further capable of storing said missed
3 cache line into said data cache.

1 6. The data processor as set forth in Claim 5 wherein said
2 cache refill controller causes said first data value to be
3 transferred to said functional unit by retrieving said first data
4 value from said missed cache line stored in said data cache.

1 7. The data processor as set forth in Claim 6 wherein said
2 cache refill controller causes said first data value to be
3 transferred to said functional unit after said cache miss via said
4 bypass circuitry.

1 8. The data processor as set forth in Claim 7 wherein said
2 clock controller generates an early clock signal when said
3 execution pipeline is stalled, wherein said early clock signal
4 causes said first data value to be transferred to said functional
5 unit from said data cache.

1 9. The data processor as set forth in Claim 8 wherein said
2 cache refill controller restarts said instruction execution
3 pipeline after said clock controller generates said early clock
4 signal.

1 10. A processing system comprising:
2 a data processor;
3 a memory coupled to said data processor;
4 a plurality of memory-mapped peripheral circuits coupled
5 to said data processor for performing selected functions in
6 association with said data processor, wherein said data processor
7 comprises:

8 an instruction execution pipeline comprising N
9 processing stages, each of said N processing stages capable of
10 performing one of a plurality of execution steps associated
11 with a pending instruction being executed by said instruction
12 execution pipeline;

13 a data cache capable of storing data values used by
14 said pending instruction;

15 a plurality of architectural registers capable of
16 receiving said data values from said data cache;

17 bypass circuitry capable of transferring a first
18 data value from said data cache directly to a functional unit
19 in one of said N processing stages without first storing said
20 first data value in a destination one of said plurality of
21 architectural registers; and

22 a cache refill controller capable of detecting that

23 a cache miss has occurred at a first address associated with
24 said first data value, receiving a missed cache line from a
25 main memory coupled to said data processor, and causing said
26 first data value to be transferred from said missed cache line
27 to said functional unit.

1 11. The processing system as set forth in Claim 10 wherein
2 said cache refill controller is further capable of stalling said
3 instruction execution pipeline after said cache miss by halting
4 clock signals driving said instruction execution pipeline.

5 12. The processing system as set forth in Claim 11 further
6 comprising a clock controller coupled to said cache refill
7 controller and capable of generating said clock signals driving
8 said instruction execution pipeline, wherein said clock controller
9 stalls said instruction execution pipeline by halting said clock
10 signals in response to a command from said cache refill controller.

1 13. The processing system as set forth in Claim 12 wherein
2 said cache refill controller causes said first data value to be
3 transferred to said functional unit when said instruction execution
4 pipeline is stalled.

1 14. The processing system as set forth in Claim 13 wherein
2 said cache refill controller is further capable of storing said
3 missed cache line into said data cache.

1 15. The processing system as set forth in Claim 14 wherein
2 said cache refill controller causes said first data value to be
3 transferred to said functional unit by retrieving said first data
4 value from said missed cache line stored in said data cache.

1 16. The processing system as set forth in Claim 15 wherein
2 said cache refill controller causes said first data value to be
3 transferred to said functional unit after said cache miss via said
4 bypass circuitry.

1 17. The processing system as set forth in Claim 16 wherein
2 said clock controller generates an early clock signal when said
3 execution pipeline is stalled, wherein said early clock signal
4 causes said first data value to be transferred to said functional
5 unit from said data cache.

1 18. The processing system as set forth in Claim 17 wherein
2 said cache refill controller restarts said instruction execution
3 pipeline after said clock controller generates said early clock
4 signal.

1 19. For use in a data processor comprising 1) an instruction
2 execution pipeline comprising N processing stages, each of the N
3 processing stages capable of performing one of a plurality of
4 execution steps associated with a pending instruction being
5 executed by the instruction execution pipeline, and 2) bypass
6 circuitry capable of transferring a first data value from a data
7 cache directly to a functional unit in one of the N processing
8 stages without first storing the first data value in a destination
9 architectural register, a method of handling a cache miss
10 comprising the steps of:

11 detecting that a cache miss has occurred at a first
12 address associated with the first data value;

13 stalling the operation of the instruction execution
14 pipeline;

15 receiving a missed cache line from a main memory coupled
16 to the data processor;

17 transferring the first data value from the missed cache
18 line to the functional unit.

1 20. The method as set forth in Claim 19 wherein the step of
2 stalling comprises the sub-step of halting clock signals driving
3 the instruction execution pipeline.

1 21. The method as set forth in Claim 20 further comprising
2 the step of storing the missed cache line into the data cache.

1 22. The method as set forth in Claim 21 wherein the step of
2 transferring comprises the sub-step of retrieving the first data
3 value from the missed cache line stored in the data cache.

1 23. The method as set forth in Claim 23 wherein the step of
2 transferring further comprises the sub-step of transferring the
3 first data value to the functional unit after the cache miss via
4 the bypass circuitry.

1 24. The method as set forth in Claim 23 further comprising
2 the step of restarting the instruction execution pipeline after
3 completion of the sub-step of transferring the first data value to
4 the functional unit after the cache miss via the bypass circuitry.